R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

Applicants' thank Examiner Chase for the indications of allowable matter in claims 4, 5, 8-10, 13-15 and 18.

SUPPORT FOR THE CLAIM AMENDMENTS

Support for the claim amendments may be found in the specification, for example, on page 17 line 12 thru page 18 line 11, FIG. 4 and claim 13, as originally filed. Thus, no new matter has been added.

DRAWING OBJECTION

The objection to FIGS. 1 and 2 has been obviated by the proposed drawing amendments and should be withdrawn. Approval by the Examiner of the proposed drawing amendments is respectfully requested. The phrase "conventional" has been added to FIGS. 1 and 2. Furthermore, the reference number 122B in FIG. 4A has been changed to 124A to agree with the text on page 12, lines 7-9.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1, 2, 6, 7 and 19 under 35 U.S.C. §102(b) as being anticipated by Itakura et al. '795 (hereafter

Itakura) has been obviated in part, is respectfully traversed in part, and should be withdrawn.

The rejection of claims 11, 13, 16 and 17 under 35 U.S.C. §102(e) as being anticipated by Ulmer et al. '126 (hereafter Ulmer) is respectfully traversed and should be withdrawn.

Itakura concerns a Viterbi decoder with path metric comparisons for increased decoding rate and with normalization timing calculation (Title). Ulmer concerns an efficient trellis state metric normalization (Title).

In contrast, claim 1 provides a state metric circuit configured to determine a normalization signal calculated from a plurality of intermediate signals. Page 4 of the Office Action asserts that a normalization command circuit 5 of Itakura discloses generating a normalization signal. However, Itakura appear to be silent regarding the normalization signal being calculated from intermediate signals found within an ACS-CM normalization circuit 4 of Itakura (asserted similar to the claimed state metrics circuit). Therefore, Itakura does not appear to disclose or suggest a state metric circuit configured to determine a normalization signal calculated from a plurality of intermediate signals as presently claimed.

Claim 1 further provides a state metric circuit configured to both (i) determine a next state metric signal and determine a normalization signal. In contrast, page 4 of the

Office Action asserts that (i) the ACS-SM normalization circuit 4 of Itakura generates the next states and (ii) the normalization command circuit 5 of Itakura generates the normalization signal. Itakura appears to discuss a different structure using two circuits where claim 1 uses a single circuit. Therefore, Itakura does not appear to disclose or suggest the structure as arranged in claim 1. As such, claim 1 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 19 provides both (i) a means for adding a plurality of branch metric signals to a plurality of state metric signals to generate a plurality of intermediate signals and (ii) a means for determining a normalization signal in response to the intermediate signals. Page 3 of the Office Action asserts that an accumulation within the ACS-SM normalization circuit 4 of Itakura discloses generation of the intermediate signals. Therefore, the Office Action appears to be asserting that signals AS1-AS4 of Itakura are similar to the claimed intermediate signals. However, Itakura appears to be silent regarding the normalization command circuit 5 generating a normalization signal in response to the AS1-AS4 signals. Therefore, Itakura does not appear to disclose or suggest (i) a means for adding a plurality of branch metric signals to a plurality of state metric signals to generate a plurality of intermediate signals and (ii) a means for determining a

normalization signal in response to the intermediate signals as presently claimed.

Claim 19 further provides both (i) a means for determining a next state metric signal to the plurality of state metrics signals in response to the intermediate signals and (ii) a means for normalizing the state metric signals in response to a normalization signal. In contrast, page 4 of the Office Action asserts that the ACS-SM normalization circuit 4 of Itakura generates the next state metrics. Therefore, the Office Action appears to be arguing that a selection-normalization portion 15 of Itakura determines the next metrics signal in response to the AS1-AS4 signals (asserted similar to the claimed intermediate signals). However, FIG. 2 of Itakura shows that the selection-normalization portion 15 receives the normalization signal from the normalization command circuit 5. Therefore, Itakura does not appear to distinguish between (i) a means for determining a next state metric signal to the plurality of state metrics signals in response to a plurality of intermediate signals and (ii) a means for normalizing the state metric signals in response to a normalization signal as presently claimed. As such, claim 19 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 6 provides that each of a plurality of state metric signals is represented by a fixed point variable. Despite the assertion on page 4 of the Office Action, Itakura does not appear

to expressly or inherently disclose fixed point variable representations. The Examiner is respectfully requested to either (i) clearly identify where Itakura expressly discloses fixed point representations, (ii) provide an explanation how receiving processed inputs from a punctured circuit inherently discloses representing state metric signals as fixed point or (iii) withdraw the rejection.

Claim 11 provides a step for adding a plurality of branch metric signals to a plurality of state metric signals to generate a plurality of intermediate signals. Despite the assertion on page 5 of the Office Action, column 5 lines 30-40 of Ulmer appear to be silent regarding adding branch metrics to state metrics:

> One or more, preferably three, state-metric (SM) calculation units 30, 32 and 34 receive the BMs and accordingly calculate the state-metrics of each of the states of the code, as described further hereinbelow. Preferably, SM calculation units 30, 32 and 34 receive the BMs from one or more memory units 28 where the branch-metrics are stored. Further preferably, each SM calculation unit has its own BM memory unit 28 so that the SM calculation units can operate in parallel without interfering with each other. Preferably, SM units 30, 32 and 34 differ in the direction in which the packet is processed. Unit 30 processes the packet in a first (forward) direction, from beginning to end, while units 32 and 34 process the packet in the opposite (reverse) direction, from end to beginning.

Nowhere in the cited text does Ulmer appear to discuss adding branch metrics to state metrics as presently claimed. Furthermore, the Office Action has failed to identify signals within Ulmer that explicitly or inherently disclose the claimed intermediate signals. Therefore, the Office Action has failed to establish *prima facie*

anticipation. As such, the Examiner is respectfully requested to either (i) identify the signals within Ulmer allegedly similar to the claimed intermediate signals or (ii) withdraw the rejection.

Claim 11 further provides a step for determining a next state metric signal of the state metric signals calculated from the intermediate signals. Page 5 of the Office Action cites column 6, lines 5-15 (talking about FIG. 3) of Ulmer as teaching the claimed step. However, nothing in the cited text or FIG. 3 of Ulmer appears to discuss determining a next state metric signal calculated from a plurality of intermediate signals. Therefore, the Office Action has failed to establish *prima facie* anticipation.

Claim 11 further provides a step for determining a normalization signal calculated from a plurality of intermediate signals. Page 5 of the Office Action appears to be arguing that (i) the combiners 50 of Ulmer disclose determining a next state metric signal and (ii) a minimum calculation unit 56 of Ulmer discloses determining a normalization signal. However, FIG. 3 of Ulmer shows that the minimization unit 56 operates on the state metrics signals SM00-SM11 generated by the combiners 50. Ulmer appears to contemplate generating a normalization signal calculated from state metric signals. In contrast, Ulmer appears to be silent regarding determining a normalization signal calculated from a plurality of intermediate signals as presently claimed. As such,

claim 11 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 12 provide determining the next state metric signal and determining the normalization signal performed in parallel. In contrast, FIG. 3 of Ulmer shows that a signal NM (asserted similar to the claimed normalization signal) is generated serially after the signals SM00-SM11 (asserted similar to the claimed next state metric signal) are calculated. Therefore, Ulmer does not appear to disclose or suggest determining a next state metric signal and determining a normalization signal performed in parallel as presently claimed. As such, claim 12 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 16 provides representing each of the state metic signals, the branch metric signals, the intermediate signals and a normalization signal as a fixed point variable. Despite the assertion on page 5 of the Office Action, column 5 lines 1-5 of Ulmer appear to be silent regarding fixed point variable representations:

> $G[D]=[1,(1+D+D^2)/(1+D)]$ (1)
> wherein D represents a delay element 12.
> FIG. 2 is a schematic block diagram of an APP decoder 20', in accordance with a preferred embodiment of the present invention.

Nowhere in the above text are state metric signals, branch metric signals, intermediate signals, a normalization signal or fixed point variable representation discussed. Therefore, the Office

Action has failed to establish *prima facie* anticipation. As such, the Examiner is respectfully requested to either (i) explain how Ulmer expressly or inherently discloses fixed point variable representations for each of the claimed signals or (ii) withdraw the rejection.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claim 3 under 35 U.S.C. §103(a) as being unpatentable over Itakura in view of Gross et al. document "Simplified MAP Algorithm Suitable for Implementation of Turbo Decoders", IEEE (hereafter Gross) is respectfully traversed and should be withdrawn.

Itakura concerns a Viterbi decoder with path metric comparisons for increased decoding rate and with normalization timing calculation (Title). Gross concerns a simplified MAP algorithm suitable for implementation of turbo decoders (Title).

Regarding claim 3, page 6 of the Office Action asserts motivation to modify Itakura with Gross is "to employ a decoding method that will reduce the decoding complexity and increase decoding speed". However, the asserted motivation is not credited to either reference or knowledge generally available to one of ordinary skill in the art. Therefore, the Office Action has failed to establish *prima facie* obviousness. As such, the Examiner is respectfully requested to either (i) identify the source of the

asserted motivation, and if knowledge generally available, provide evidence or (ii) withdraw the rejection.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.

Christopher P. Maiorana
Registration No. 42,829

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c/o Sandeep Jaggi
LSI Logic Corporation
1621 Barber Lane, M/S D-106 Legal
Milpitas, CA 95035

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